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Forward Error Correction Techniques Using VLSI

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Abstract: **Forward – Error – Correction techniques correct errors at the receiver end of digital communications systems. In contrast with error detection and retransmission techniques, FEC requires only a one-way link, and its parity bits target both error detection and correction. In most wireless communication system, convolutional coding is the preferred method of forward error correction to overcome transition distortions. In this thesis I have implemented a complete structure of channel codec (Convolutional Encoder and Viterbi Decoder). The codec is designed for two different code rates. The encoder encodes the input data and transmits it serially over a wire channel and decoder decodes it to reconstruct the original information. The channel encoder uses Convolutional Encoder of type (2,1,2) or (3,1,2). Encoding of the data is done using shift register and modulo – 2 adder. To decode the data Viterbi algorithm is used which uses Trellis to decode data. The received data bits are first compared with the Trellis Branch Word and minimum Hamming distance path is selected as Survivor path. As we need Trellis for Decoder, to reduce the memory requirement instead of storing Trellis to calculate Branch Metric it is generated logically in this thesis. As well as reduce the switching loss of power instead of using register for each stage only four registers for each state are used to store the output data. No retracing of survivor path is required which thereby reduces memory requirement, power consumption and time required for getting decoded output.**

I. INTRODUCTION

Over the years, there has been a tremendous growth in digital communications especially in the fields of cellular/PCS, satellite, and computer communication. In these communication systems, the information is represented as a sequence of binary bits. The binary bits are then mapped (modulated) to analog signal waveforms and transmitted over a communication channel. The communication channel introduces noise and interference to corrupt the transmitted signal. At the receiver, the channel corrupted transmitted signal is mapped back to binary bits. The received binary information is an estimate of the transmitted binary information. Bit errors may result due to the transmission and the number of bit errors depends on the amount of noise and interference in the communication channel.

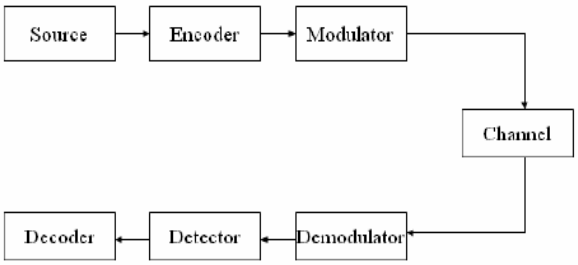


Figure 1.1: Digital Communication System

1.1.1 Types of Channel Coding

Convolution coding and block coding are two major forms of channel coding. Block codes operate on relatively large message blocks. Convolution codes operate on serial data, one or a few bits at a time [6].

Block Codes

Early attempts at designing error control techniques were based on block codes. For every block of k information bits, n-k redundant parity-check bits are generated as linear (modulo-2) combinations of the information bits and transmitted along with information bits as a code of rate k/n bits/symbol. These can be generated by means of a linear feedback shift register encoder. Error detection can be easily implemented with any parity-check block code.

Convolutional Codes

Convolution coding with Vertebra decoding is a FEC technique that is particularly suited to a channel in which transmitted signal is corrupted mainly by additive white Gaussian noise (AWGN) [6]. In most of real time applications like audio and video applications, the convolutional codes are used for error correction.

The Viterbi algorithm is an optimum decoding technique. It is optimum as it results in the minimum probability of error. It is also the relatively straight algorithm to implement in hardware and is the best decoding technique. Viterbi algorithm is a maximum likelihood algorithm and performs decoding, through searching the minimum cost path in a weighted oriented graph, called trellis. The basic building blocks of Viterbi decoder are branch metric unit (BMU), path metric unit (PMU), add compare and select unit (ACSU) and survivor memory management unit (SMU).

II. Proposed Architecture For The Channel Codec

Below, I present the circuit diagrams of the encoder, decoder and their subsequent sub-blocks.

2.1 Encoder blocks schematic:

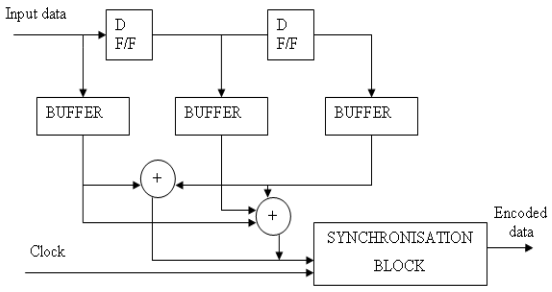


Figure 2.1: Encoder block schematic

Description:

For above (2, 1, 2) encoder

- N=2, for each input bit we get 2 encoded bits at the output.
- K=2, constraint length is 2.

The diagram of convolutional (2,1,2) encoder is shown in figure 3.1. The encoder is a simple shift register consists of D flip-flops. The outputs of the each flip-flop are connected to EX-OR gates according to generator polynomial equation. The message bits are applied to the input of the shift register. The decoded bit stream is obtained at the output.

2.1.1 Convolution Encoder:

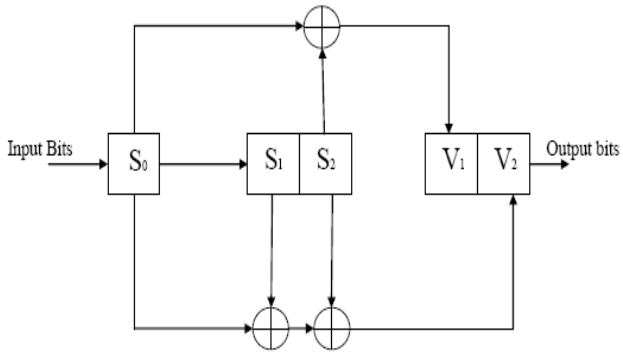


Figure 2.2: Convolution Encoder block schematic

A convolutional coding is done by combining the fixed number of inputs bits. The input bits are stored in the fixed length shift register and they are combined with the help of mod-2 adders.

V1 = S0 XOR S1 and
V2 = (S0 XOR S1) XOR S2

2.2 Decoder blocks schematic**:**

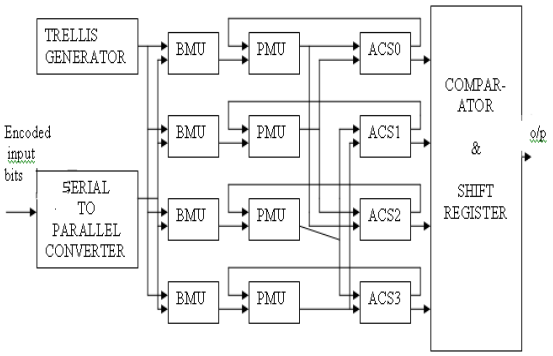


Figure 2.3: Decoder block schematic

The receiver receives the serial encoded data and converts it into 2-bit parallel data. This parallel data is now feed to the subsequent blocks. Trellis Generator generates the predefined sequence, which is used to calculate the branch metric unit.

III. Simulation Results

1.1 Block Diagram:

Transmitter (ENCODER):

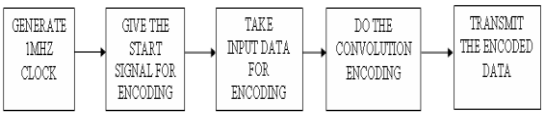


Figure 3.1: Block Diagram of Encoder

Receiver (DECODER):

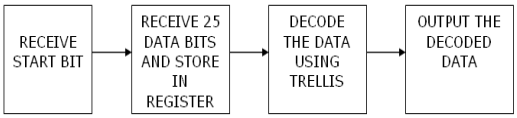
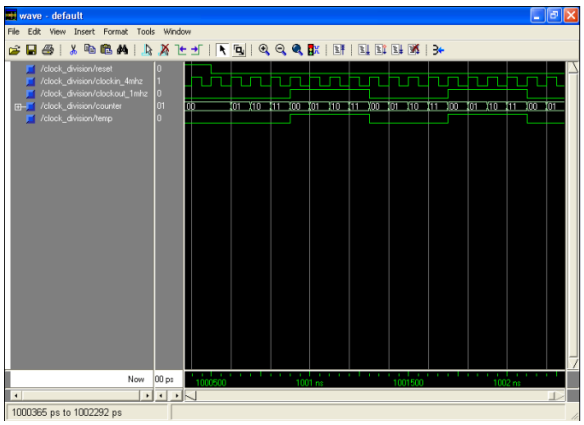
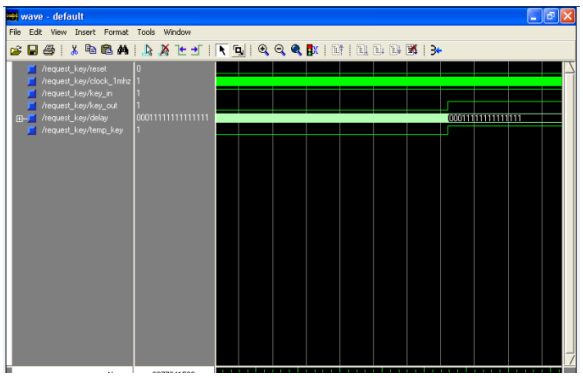


Figure 3.2: Block Diagram of Decoder

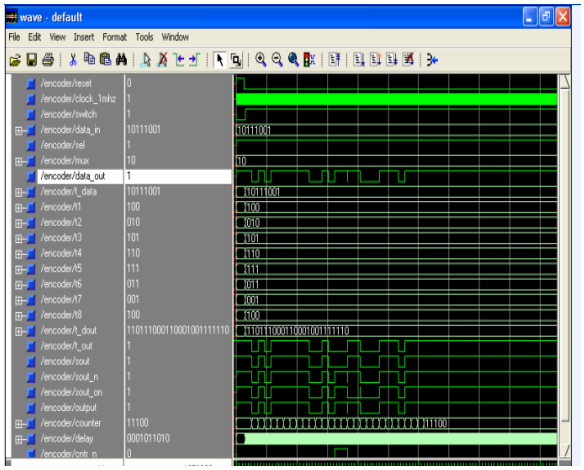
OUTPUT OF CLOCK DIVISION



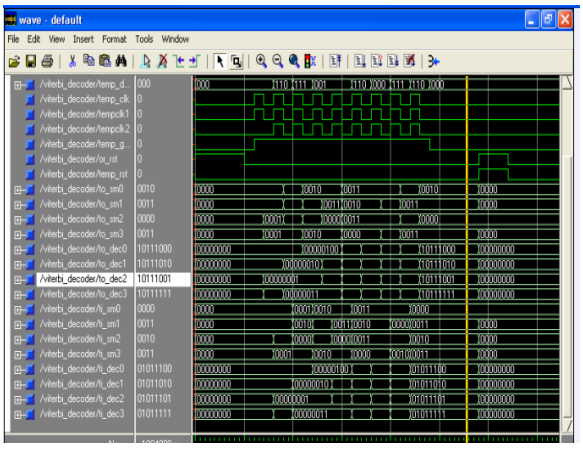
OUTPUT OF REQUEST KEY



OUTPUT OF ENCODER
(Code rate: 1/3)

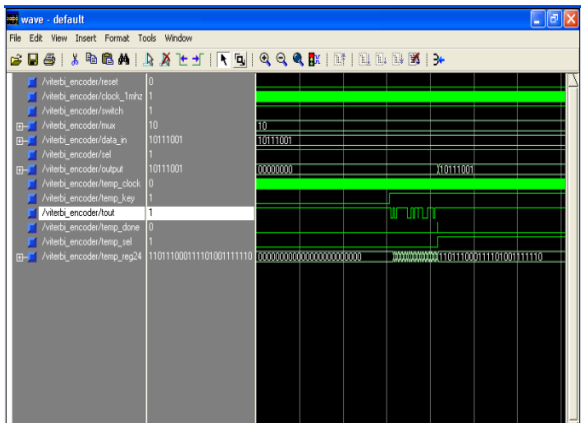


OUTPUT OF DECODER



ENCODER DECODER FINAL OUTPUT

Code rate: 1/3, mux: 10
Data transmission with low noise



IV. CONCLUSION

The complete structure of channel codec (Convolutional Encoder and Viterbi Decoder) is described in the dissertation. Viterbi Decoders employed in digital communication are complex and dissipate high power. The design explained in the dissertation requires the less hardware. This reduces switching loss as well as the power loss. As the traceback approach is not use time required is also less as compared to traceback method. Memory required is also less.

The Design is finally implemented the following FPGA Devices:

1. Device: Spartan2, xc2s200-5pq208
2. Device: Virtex, XCV100-4pq240

Virtex device is better than spartan2 because of less hardware required, faster.

This architecture with its significant reduction of hardware complexity is very attractive for wireless applications such as CDMA and WLAN systems.

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